IN THE CLAIMS

1. (Currently Amended) A method for recovering from data errors within a processor, comprising the steps of:

storing a ~~backup~~ copy of data ~~for~~ from a register of a register file ~~and~~ within a buffer prior to architecting new data in the register;

periodically checking for data errors within the processor; and

restoring the data from the buffer to the register file in the event of data errors.

2. (Canceled)

3. (Currently Amended) A method of claim 1, further comprising loading the new data to the register ~~and~~ after the step of storing.

4. (Currently Amended) A method of claim 1, further comprising loading the new data to the register ~~and~~ concurrently with the step of storing.

5. (Original) A method of claim 1, the step of storing the data within the buffer comprising storing the data within a second register file.

6. (Original) A method of claim 1, further comprising the step of flushing the buffer after checking for, and detecting no, data errors.

7. (Original) A method of claim 1, further comprising the step of freezing execution of instructions within pipelines of the processor after detecting data errors.

8. (Currently Amended) A method of claim 1, further comprising the step of ~~backing up~~ resetting a program counter of the processor after detecting errors.

9. (Currently Amended) A method of claim 8, further comprising ~~the~~ a step of re-executing a program through the processor at a time associated with the ~~backed up~~ reset program counter.

10. (Original) A method of claim 1, the step of periodically checking for data errors comprising periodically checking for the data errors at sequential time periods defined by a number of processor clock cycles.

11. (Original) A method of claim 1, further comprising the steps of utilizing an error correction code in connection with data storage to the buffer.

12. (Currently Amended) A processor with register file data recovery, comprising:

an execution unit having a plurality of pipelines for processing program instructions relative to a program counter;

a register file, wherein one or more stages of the pipelines loads data to a register of the register file; and

a buffer for storing a ~~backup~~ copy of data within the register and for restoring data to the register file in the event of data errors within the processor.

13. (Original) A processor of claim 12, the buffer comprising a second register file.

14. (Original) A processor of claim 12, the register file comprising an extra read port for reading the data from the register.

15. (Original) A processor of claim 12, the register file comprising a write port for writing the data from the buffer to the register.

16. (Original) A processor of claim 12, further comprising one or more error detectors for detecting the data errors.

17. (Original) A processor of claim 16, the error detectors comprising redundant logic devices.

18. (Original) A processor of claim 12, further comprising error correction code for data recovery of data stored within the buffer.

19. (Original) A processor of claim 12, the buffer reading data within the register prior to an execution stage for an instruction identifying a write to the register.

20. (Currently Amended) A processor of claim 12, ~~further comprising a program counter,~~ wherein the program counter being reset in connection with the buffer restoring data to the register file.